INVESTIGATION OF SHORT CHANNEL EFFECT ON VERTICAL STRUCTURES IN NANOSCALE MOSFET

Munawar A. Riyadi[1], Ismail Saad[2], Razali Ismail[3]
[1]Department of Electrical Engineering, Diponegoro University, Semarang 50275, Indonesia
[2]School of Engineering & IT, Universiti Malaysia Sabah, 88999, Kota Kinabalu, Sabah, Malaysia
[3]Faculty of Electrical Engineering, Universiti Teknologi Malaysia, 80310 Skudai, Johor, Malaysia
*Corresponding author: munawar.riyadi@ieee.org

Abstrak

Perkembangan MOSFET yang terkini memerlukan pendekatan inovatif untuk mempertahankan tren miniaturisasi ke dimensi nano. Makalah ini memfokuskan pada sifat fisik MOSFET vertikal dalam ukuran nano. Struktur vertikal adalah salah satu jenis devais yang menjanjikan untuk miniaturisasi lebih lanjut, dengan fitur yang tidak terikat dengan lithografi dalam pembuatannya. Perbandingan kinerja MOSFET vertikal dan lateral untuk panjang kanal Lch berukruan nano ini ditunjukkan dengan bantuan perhitungan numerik. Evaluasi parameter-parameter efek kanal pendek (short channel effect-SCE), yaitu penurunan tegangan ambang batas, subthreshold swing (SS), drain induced barrier lowering (DIBL) dan arus bocor menunjukkan keuntungan yang cukup besar, serta beberapa pertimbangan dalam menerapkan struktur tersebut, khususnya untuk ukuran nano.

Kata kunci: *efek kanal pendek, MOSFET vertikal, nanoscale device, pabrikasi*

Abstract

The recent development of MOSFET demands innovative approach to maintain the scaling into nanoscale dimension. This paper focuses on the physical nature of vertical MOSFET in nanoscale regime. Vertical structure is one of the promising devices in further scaling, with relaxed-lithography feature in the manufacture. The comparison of vertical and lateral MOSFET performance for nanoscale channel length (Lch) is demonstrated with the help of numerical tools. The evaluation of short channel effect (SCE) parameters, i.e. threshold voltage roll-off, subthreshold swing (SS), drain induced barrier lowering (DIBL) and leakage current shows the considerable advantages as well as its thread-off in implementing the structure, in particular for nanoscale regime.

Keywords: fabrication, nanoscale dimension, short channel effect, vertical MOSFET

1. INTRODUCTION

The recent development of MOSFET has reached the progress that the channel length goes shorter into nanometer scale. While the MOSFET undergoes scaling down of the size in order to improve integrated circuit performance such as speed, power consumption, and packing density, a number of challenges need to be overcome. This improvement in device speed and the shrinking of dimensions has continued successfully for over 30 years, as predicted by Moore's Law more than 40 years ago[1]. While the performance and density of the device is expected to be higher with the shrinking of the gate length, some challenges on the ordinary, lateral MOS device arose [2]. This dimension reduction has the biggest impact on lithography, as the key equipment for transferring design features onto substrate. When the device resolution goes smaller, it gives the consequences for the use of lithography source wavelength. As a rule of thumb, the resolution of lithography is about half of the wavelength of its source [3]. Thus, with channel length goes into sub-100 nm in length, the lithography had to be into deep UV or even in the x-ray region, which eventually lead to more expensive and sophisticate equipment installment. With it, the cost of manufacturing and also its complexity tend to increase dramatically. Other challenges over the channel scaling are the short channel effects. The short channel effect includes threshold voltage reduction, increasing dissipation

power, I_{off} roll-off and drain induced barrier lowering (DIBL) [4]. As a result, alternative technologies are essential as well as advanced device physics approach for overcoming these challenges.

A number of research have been conducted extensively to overcome the problem in further scaling, including the research in new materials (high-k for gate dielectric, for instance) and new device structures [5-10]. The vertical transistors have been recognized as potential solution in overcoming the scaling problems due to lithography resolution in which decananometer channels can be realized with the accuracy of ion implantation or epitaxial growth[11, 12]. A vertical MOSFET structure has its source, channel and drain arranged vertically, usually using a silicon pillar. Its channel region locates at the sidewall surface of the pillar. By this structure, the gate length definition is independent of lithography but only depends on the very well controlled vertical processing, e.g. pillar etching, thin film deposition or growth. Another possible advantage is the increased packing density as the channel width is large because of the usage of all sidewalls as channel region [13]. With the need to reduce the channel length, advancement in fabrication techniques was essential for the suppression of unwanted phenomena.

In this paper, the comparison of lateral and vertical MOSFET's performance will be presented. This paper will concentrate on single gate vertical structure compared to its lateral counterpart, different than the approach of vertically double gate transistor [14]. The solid source diffusion technique was selected in this review for its simplicity in structure and processing. In addition, its behaviour over schort channel effect will be discussed extensively by the help of numerical analysis using Silvaco technology computer-aided design (TCAD) software.

2. DEVICE STRUCTURE AND PHYSICAL MODELS

Figs. 1(a) and (b) show the basic structure of vertical and lateral MOSFET, respectively. Only one side of the vertical Si pillar is simulated, while usually both side are used, for the one-to-one comparison between the lateral and vertical structure. From this picture it is obvious that the channel is located vertically between drain and source (Fig. 1(b)), and that the definition of channel region for vertical MOSFET is lithography-independent.

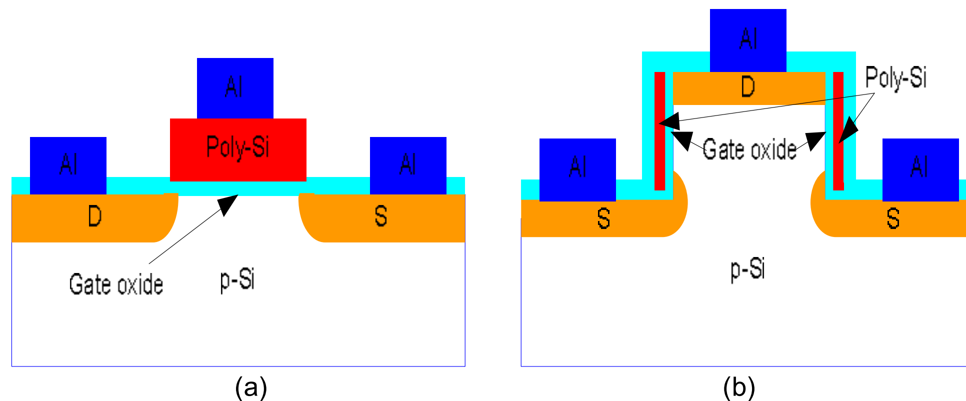

Fig. 1 The concept of (a) lateral and (b) vertical MOSFET

Silicon wafer with uniform boron doping of 10^{18} cm^{-3} is used as base substrate for both structures. The use of relatively high substrate doping is a consequence of device scaling which requires higher substrate doping for shorter gate length. In addition, it also gives benefit for the suppression of short channel effect [4]. A 5-nm Silicon oxide (SiO_2) is grown on the substrate as a gate dielectric, while polysilicon which is heavily doped with arsenic of 10^{19} cm^{-3} is applied for gate electrode. The polysilicon gate was also used as masker for self-aligned source and drain region for lateral structure, while no self-aligned process is in the vertical. The source and drain region was constructed by doping of phosphorus with concentration of 10^{20} cm^{-3}. Aluminum was

used as metal contact, and ohmic contact was assumed between metal and semiconductor. The lateral structure was designed using standard MOSFET processing sequence. In other hand, the vertical structure has additional processing steps to standard sequences, with the requirement of the trench (pillar) definition. In order to obtain clear cut pillar, isotropic etch was applied for this purpose. The height of the pillar is adjusted with the targeted channel length, and also by determining the required space for drain impurity diffusion junction.

The device structure was then simulated using SILVACO's ATLAS software package [15]. Several channel lengths were simulated to understand the performance and characteristic of the devices. For the purpose of comparison study based on identical models for both devices the analysis on I-V characteristics and secondary effects are to be captured well. The Lombardi model [16] was applied as it has taken into account the mobility degradation occurs inside inversion layers through transverse and longitudinal field. In a low electric field, the carrier mobility is given using Matthiessen's rule as

$$\mu_T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1} \quad (1)$$

μ_{AC} is the surface mobility limited by scattering with acoustic phonons given by

$$\mu_{AC} = \frac{B}{E_{\perp}} + \frac{C N^{\frac{1}{8}}}{T_L E_{\perp}} \quad (2)$$

where $B = 4.75 \times 10^7$ cm/s, $C = 1.74 \times 10^5$, N is total doping concentration, $E_{\perp}$ transverse field and T_L is lattice temperature in Kelvin. μ_b is the mobility limited by scattering with optical intervalley phonons given by

$$\mu_b = \mu_0 + \frac{\left(\mu_m (T_L/300)^{-2.5} - \mu_0\right)}{1 + (N_A/C_r)^{0.680}} - \frac{\mu_1}{1 + (C_s/N_A)^2} \quad (3)$$

$$\mu_{sr} = \delta / E_{\perp}^2 \quad (4)$$

where μ_0 = 52.2 cm^2/(V.s), μ_m=1417 cm^2/(V.s), μ_1 = 43.4 cm^2/(V.s), $C_r = 9.86 \times 10^{16}$ cm^{-3}, $C_s = 3.43 \times 10^{20}$ cm^{-3}, N_A is the total density of impurities, μsr the surface roughness factor for electrons and δ =5.82x10^{14} cm^2/(V.s). The mobility degradation due to present of electric field is given by the relation

$$\mu_n(E_{\parallel}) = \mu_{n0} \left[1 / \left(1 + \left(\mu_{n0} E_{\parallel} / V_{SATN} \right)^{\beta} \right) \right]^{\frac{1}{\beta}} \quad (5)$$

where μ_{n0} is the electrons low-electric-field mobility and $E_{||}$ is the longitudinal electric field in the direction of current. V_{SATN} is the saturated drift velocity calculated from temperature-dependent model[17].

The recombination behaviors between electrons and holes are described by Shockley-Read-Hall equation with fixed carrier lifetimes. An interface fixed oxide charge of 3×10^{10} C/m^2 is assumed with the presence of n-type polysilicon gate. The combination of Gummel and Newton numerical methods was employed for a better initial guess in solving quantities for obtaining a convergence of the device structure.

3. RESULTS AND DISCUSSION

The device's electrical properties were extracted primarily for the analysis of short channel effect. The effect of structure on the threshold voltage is shown in Figure 2. The result shows tendency of decrease in threshold voltage for decreasing channel length for both structure, while V_{th} decreases more dramatically below 100 nm. The threshold voltages of vertical structure are generally higher than that of lateral, however the roll-off tendency (i.e. the rate of threshold decrease in lower channel length) for both graphs indicate that vertical structures are more likely to have better control of threshold roll-off. Worse roll-off is a sign of less control for channel, and eventually it can lead to negative threshold voltage, which requires complicated bias setup for its operation.

The value of V_{th} is critical for switching operation, and especially for determining the operating region of transistor's OFF-state, which obviously lies below threshold voltage. While V_{th} goes higher, the corresponding off-voltage could be set more flexible, and eventually the off current (I_{off}) will be lower. But if the threshold voltage tends to be low, the off-voltage would be forced to go lower, and tend to increase the instability of switching operation. Later, this will lead to higher I_{off}, and considerably the higher power consumption at off state. However, higher V_{th} could set the operating voltage at higher bias, thus it can pull the power higher in on-state. By comparing the result with recent IC manufacturing technology provided by ITRS [18], it can be seen that the threshold voltage of sub-100 nm is maintained in the order of 0.5 V. Thus, the obtained value of V_{th} for vertical structure (Fig. 1) is acceptable.

In the presence of high electric field i.e. V_d between source and drain, its respective potential barrier can be affected which leads to an increased drain current, and eventually changes its threshold voltage. This parasitic effect is known as drain induced barrier lowering (DIBL), which is calculated by:

$$DIBL = \Delta V_{th} / \Delta V_d \tag{6}$$

The DIBL calculation is taken for V_{th} at V_D = 0.1 V and V_D= 1.0 V, as is presented in Fig. 3. It is shown that the lateral structure has the tendency of lower DIBL for channel length above 100 nm, while the vertical offers better trend of DIBL for sub-100 nm length. This means that the vertical structure could stand for higher drain current in shorter channel with less current consumption and threshold voltage than the lateral.

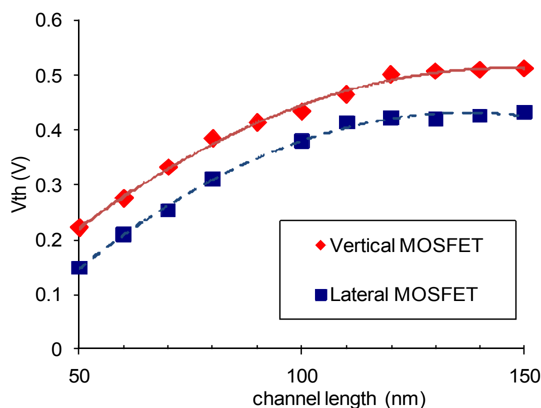

Fig. 2 Comparison of threshold voltage (V_{th}) between lateral and vertical structure

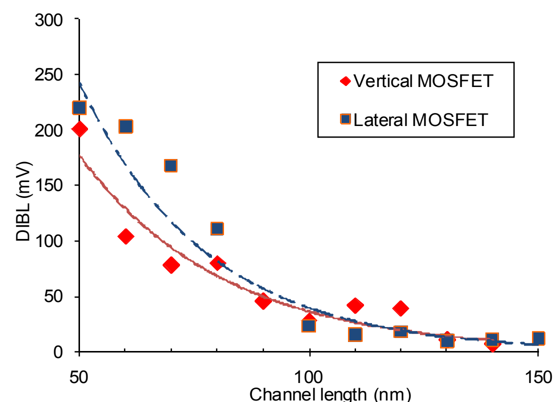

Fig. 3 Trend of DIBL for lateral and vertical MOSFET

The subtreshold swing (S) of both lateral and vertical structures is shown in Fig.4 (a). The swing is used to reflect the transition speed of device from weak to strong inversion region, as shown below:

$$S = \frac{kT}{q}\ln 10.\left(1 + \frac{C_d + C_{it}}{C_{ox}}\right) \quad (7)$$

where k is Boltzmann's constant, T is temperature, and $C_{d,}$ C_{it} and C_{ox}, are the depletion, interface trap and oxide capacitances, respectively. The interface trap capacitance is equal to qD_{it}., where D_{it} is the interface trap density. Low swing reflects a good transition time, thus lower S value is preferable. Due to the bulk effect the sub-threshold swing of a conventional MOS transistor in bulk technology will always be higher than a certain optimum value which is roughly 60 mV/dec at room temperature.

The vertical structure gives lower subthreshold swing for overall simulated channel lengths at around 90 mV/dec. On the other hand, lateral structure has its swing rose sharply below 80 nm, although both structures have similar oxide capacitance. The depletion capacitance is considered as the influential part for the increased swing, as the lateral locate its depletion region over all junctions in the bulk, including some part of channel, whilst in vertical structure, the narrow pillar become a constraint for depletion region. In addition, the 'depth' of junction in vertical structure (see Fig.1 (b)) is essentially shallower than that of the lateral. Thus, the transition to inversion region will be faster in vertical case.

Fig. 4(b) demonstrates the leakage current of both structures. The value of I_{off} was taken for V_g = 0V and minimum drain voltage to suppress any high electric field. It can be seen that the vertical structure have lower I_{off} than that of lateral for all channel length by some order of magnitude. The off-current increases for decreasing channel length, with the lateral structure rises more steeply in shorter channel. This confirms the phenomena of decreasing threshold voltage, as noted before. Physically, in short-channel devices the source and drain will also control of the depletion charges as well as the gate. The shared charges affected by source and drain will occupy a large fraction of total depletion charge, and later make a shift in V_{th} when the gate length is decreased. While the tendency of Vth decreasing in reduced channel length is inevitable [4], the degree of reduction is the matter of concern, as it will reflects the immunity of shorter channel effect, and thus prevent the dramatically increasing power consumption, especially in off-state region.

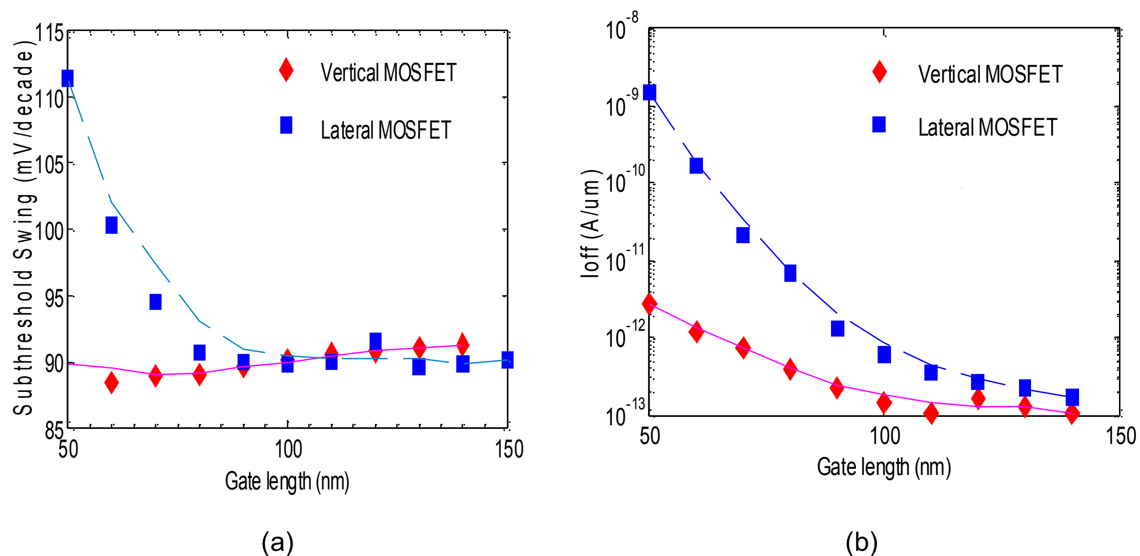

Fig. 4 (a) Subthreshold swing (SS) of vertical and lateral MOSFET for channel length= 50-150 nm, and (b) the leakage current (I_{off}) of both structures (taken at V_g=0V)

4. CONCLUSION

The performances of MOSFET for different structures and channel dimensions have been demonstrated using the TCAD tools. The vertical structure of MOSFET is found to have better performance than that of the lateral, especially for its excellent threshold voltage and low

leakage current, by several orders of magnitude. While the subtreshold swing for both structures were found to be greater than the ideal value (i.e. 60 mV/decade), the tendency of vertical structure showed that it would give smaller variation than that of lateral for channel length below 100 nm. The value of DIBL for vertical structure is lower for channel length below 100 nm, which showed the ability to stand in higher drain current than that of lateral. As a result, the vertical structure offers better performance in shorter channel. It would also reduce power consumption and provides a good control of SCE than the lateral, especially for nanoscale devices.

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